SEMICONDUCTOR PACKAGE INCLUDING TOP-SURFACE TERMINALS FOR MOUNTING ANOTHER SEMICONDUCTOR PACKAGE

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CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation-in-part of U.S. Patent Application "INTEGRATED CIRCUIT SUBSTRATE HAVING LASER-EMBEDDED CONDUCTIVE PATTERNS AND METHOD THEREFOR", Serial number 10/138,225 filed on May 1st, 2002 by at least one common inventor and assigned to the same assignee. The specification of the above-referenced Patent Application is herein incorporated by reference.

FIELD OF THE INVENTION

The present invention relates generally to semiconductor packaging, and more specifically, to a semiconductor package having top-surface grid array terminals for mounting another semiconductor package.

BACKGROUND OF THE INVENTION

Semiconductor packages that provide mechanical mounting and electrical interconnection of a semiconductor die are commonly provided in ball grid array and land grid array configurations.

A semiconductor die is electrically connected to a substrate with a grid array terminals disposed on the "bottom" side of the semiconductor package and solder balls are attached for connection to a system substrate, typically a printed circuit board (PCB) having lands located to attach the solder balls of the semiconductor package (referred to as ball grid array or BGA attach). Alternatively, conductive paste, a socket or "interposer" may be used to provide contacts between lands of the semiconductor package and lands on the system substrate (referred to as land grid array or LGA connection).

Typical system interconnect of grid array type packaging is generally two-dimensional. That is, multiple grid array devices are mounted on a PCB in different locations along the surface of the PCB and interconnected via circuit traces on or within the PCB. Such mounting is suitable for small, thin assemblies, but when the area of a PCB is of concern in a design, or in systems where other components are much taller than the semiconductor packages are present, it would be desirable to require less circuit board area by stacking semiconductor packages.

Specific semiconductor packages used for implementing three-dimensional stacked packages are well known in the art. However, such packaging is typically not compatible with existing integrated circuit packages, so that two or more

integrated circuits that are "stacked" must all be designed for stacking.

Also, when combining multiple semiconductor packages in an assembly, at times it is advantageous to permit removal or at least of one semiconductor package, so that when one semiconductor package is used with one of multiple alternative other semiconductor packages in a three-dimensional configuration, the interconnect between a semiconductor package may be standardized and so that one of the semiconductor packages may be removed and replaced without removing the other.

Therefore, it would be desirable to provide a semiconductor package that facilitates stacking of grid arrays and a method of manufacturing such a semiconductor package. It would further be desirable to provide such a package that provides mounting of another grid array or other semiconductor package that is removable and that may be interchangeably standardized.

SUMMARY OF THE INVENTION

The above objectives are accomplished in a semiconductor package having terminals on the semiconductor package top surface for mounting and electrically connecting to terminals of a piggybacked semiconductor package and method for manufacturing the semiconductor package. The semiconductor package includes a semiconductor die mounted on a substrate and an encapsulation

covering the semiconductor die and at least the top surface of the substrate. Multiple terminals are provided on a top surface of the encapsulation for attachment of the piggybacked semiconductor package, which may be a standard ball grid or land grid array package.

The top-surface terminals may be top surfaces of vias formed through the encapsulation by laser-ablation or other mechanism and filled with conductive paste or a low melting-temperature alloy or plated. The vias may have a conical profile to improved plating uniformity. The vias may terminate on the substrate circuit pattern, on electrical terminals on the top surface of the semiconductor die, or may pass through the encapsulation and the substrate to provide lands for bottom-side terminals.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a pictorial diagram depicting a cross sectional side view of a semiconductor package for forming a modified semiconductor package in accordance with an embodiment of the invention;

Figure 1B is a pictorial diagram depicting a cross sectional side view of the semiconductor package of Figure 1A after via holes have been formed;

Figure 1C is a pictorial diagram depicting a cross sectional side view of the semiconductor package of Figure 1B after vias are filled;

Figure 2A is a pictorial diagram depicting an electronic assembly in accordance with an embodiment of the present invention;

Figure 2B is a pictorial diagram depicting an electronic assembly in accordance with another embodiment of the present invention; and

Figure 2C is a pictorial diagram depicting an electronic assembly in accordance with yet another embodiment of the present invention.

The invention, as well as a preferred mode of use and advantages thereof, will best be understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein like reference numerals indicate like parts throughout.

DETAILED DESCRIPTION

The present invention concerns a semiconductor package and a method for manufacturing a semiconductor package that provide for top mounting of another semiconductor package in a "piggyback" configuration. While the exemplary embodiments depict ball grid array packages mounted atop a plurality of

lands on the top side of a modified semiconductor package, it should be understood by those skilled in the art, that the techniques of the present invention can be extended to other types of semiconductor interconnects.

Referring now to Figure 1A, a semiconductor package 10A for forming a semiconductor package and corresponding to a first illustrated step of manufacture is depicted. Semiconductor package 10A is in the form of a ball grid array (BGA) or land grid array (LGA) package as is commonly known in the art, except that particular circuit features are positioned for providing vias to the top side of semiconductor package 10A in subsequent manufacturing steps, so that another semiconductor package may be mounted atop semiconductor package 10A.

Semiconductor package 10A includes a die 16 mounted to a substrate 14A that includes lands 18 to which solder ball terminals may be attached or that may be connected with a conductive paste to form a LGA mounted semiconductor package. Encapsulation 12A surrounds die and substrate 14A, although substrate 14A may alternatively be exposed on a bottom side of semiconductor package 10A. Electrical connections 15 of die 16 are connected to circuit patterns 17 on substrate 14A via wires 19, but the type of die mounting is not limiting, but exemplary and other die mounting types may be used such as flip-chip die mounting. Additionally, while substrate 14A is depicted as a

film or laminate-type mounting structure, lead frame and other substrate technologies may be used within the structures of the present invention.

Referring now to Figure 1B, a first modification to semiconductor package 10A that illustrates a second step in the manufacturing process to form semiconductor package 10B is shown. Semiconductor package 10B includes a plurality of via holes 20A, 20B and 20C laser-ablated through encapsulation 12A of Figure 1A to form encapsulation 12B. While only three via holes are shown, many vias holes will be provided, generally in the form of a grid array for mounting a second BGA/LGA package atop the semiconductor package. The three via holes shown illustrate the three different types of via holes that may be provided through control of laser energy and exposure time. The first via hole type, illustrated as via 20A, is fabricated by laser-ablating either completely through semiconductor package 10B or by laser-ablating through encapsulation 12A to the top side of lands 18, so that a connection is provided through from the top side of semiconductor package 10B to the bottom side of semiconductor package 10B when the via is filled. If via 20A is ablated completely through, then the corresponding land 18 is provided by the bottom surface of a via formed in hole 20A.

The next type of via hole is provided by laser-ablating through encapsulation 12A to reach circuit pattern 17 to that

connection may be made through substrate 14A circuit patterns to die 16 electrical terminals, to lands 18 or both. The last type of via is provided by laser-ablating through encapsulation 12A to reach electrical connections 15 of die 16 so that direct connection to the circuits of die 16 can be made from a piggybacked semiconductor package. Each of via holes 22A, 22B and 22C is depicted as a via hole having a conical cross-section, which is desirable for providing uniform plating current density during a plating process. However, via holes 22A, 22B and 22C may alternatively be made cylindrical in shape if the advantage of cylindrical cross-section is not needed, for example if a conductive paste is used to fill the via holes.

Referring now to Figure 1C, a semiconductor package 10C is illustrated forming a complete LGA package. Conductive material is applied within via holes 20A, 20B and 20C to form conductive vias 22A, 22B and 22C through encapsulation 12C and optionally substrate 14C for vias that are formed completely through substrate 14C. The conductive material used form vias 22A, 22B and 22C may be electroplated or electro-less plated metal, conductive paste such as copper or silver epoxy compounds, or a low melting temperature high-wicking solder alloy such as SUPER SOLDER.

Referring now to Figure 1D, a semiconductor package 10D is illustrated forming a complete BGA package. Solder balls 24 are

attached to lands 18 to provide the BGA terminals used to connect semiconductor package 10D to a system substrate, such as a PCB.

Referring now to Figure 2A, an electronic assembly 30 in accordance with an embodiment of the invention is depicted. Electronic assembly 30 includes a base semiconductor package 32 as formed by the above-described process that includes through-to-land vias 34 to lands 31 and through-to-substrate vias 34A provided that contact the conductive pattern 35 on the top side of the substrate. A piggybacked second semiconductor package 36, of BGA design, is attached via solder balls 38 that provide connection to the tops of vias 34 and 34A and connect the terminals of semiconductor package 36 to internal circuits of base semiconductor package 32 or to isolated terminals 37 provided on the bottom side of base semiconductor package 36. The piggyback mounting configuration provides advantages over custom-designed three dimensional packaging, as semiconductor package 36 may be a standardized part or a part having a design not under the control of a maker of base semiconductor package 32 and therefore the provision of a top side BGA/LGA pattern on base semiconductor package 32 makes it possible to stack a pre-designed standard BGA/LGA package. Also, even when control of the design of semiconductor package 36 is possible, use of a standardized layout such as BGA/LGA provides compatibility with

standard PCB package attach layouts where semiconductor package 36 may also be used in a board mounted configuration without piggybacking.

Referring now to Figure 2B, an electronic assembly 40 is shown in accordance with another embodiment of the invention. Vias 44 are provided through to electrical connections 43 of die 41, providing a direct interface from the circuits of die 41 to circuits within piggybacked semiconductor package 46. Attachment of semiconductor package 46 is made via solder balls 48 where semiconductor package 46 may be a standard BGA package or a custom package layout designed to interface with electrical connections 43 of die 41. The depicted configuration is especially useful where short physical connections from a first semiconductor package 42 must be provided to a second interchangeable semiconductor package 46.

Referring now to Figure 2C, an electronic assembly 50 is shown in accordance with another embodiment of the invention. Vias 54 are provided through to electrical connections 53 of die 41, providing a direct interface from the circuits of die 51 to circuits within piggybacked semiconductor die 56, which is depicted as a flip-chip die. Attachment of semiconductor die 56 is made via solder balls 58 (or alternatively posts) where semiconductor die 56 is custom package layout designed to interface with electrical connections 53 of die 51. The depicted

configuration is especially useful where die 56 is one of several interchangeable dies that may be used to upgrade or provide options for use with die 53. An optional encapsulation 57, is depicted as deposited over die 56.

In addition to the die electrical connection interface depicted in Figure 2C, through-to-land or through-to-substrate circuit pattern vias may also be used to connect a die such as flip-chip die 56 directly to terminals of base semiconductor package 52 or circuit patterns on an internal substrate. Such configurations provide the advantages of three-dimensional stacking without requiring direct connection to a die within base semiconductor package 52.

The above description of embodiments of the invention is intended to be illustrative and not limiting. Other embodiments of this invention will be obvious to those skilled in the art in view of the above disclosure and fall within the scope of the present invention.